REMARKS

Claims 56 – 83 are presently pending. In the above-identified Advisory Action, the Examiner once again rejected Claims 56 – 58, and 60 – 82 under 35 U.S.C. §102(b) as being anticipated by Cake *et al.* ('121) hereinafter Cake. Claim 59 was rejected under 35 U.S.C. §103(a) as being unpatentable over Cake in view of Cheng ('428). Claim 83 was rejected under 35 U.S.C. §103(a) as being unpatentable over Cake in view of Watson ('322).

By this paper, Applicant has amended Claim 56 and submitted new Claims 85 - 107 for consideration.

For the reasons set forth more fully below, the subject application is deemed to properly present claims patentable over the prior art. Reconsideration, allowance and passage to issue are respectfully requested.

As mentioned in the Background of the subject application:

> "A highly precise current switch is needed for current switching of continuous-time analog to digital converters (ADCs) employed in delta-sigma modulators. A simple differential pair of transistors driven by a clocked latch has been used in the past to provide current switching for ADCs used in delta-sigma modulators. However, simple differential pair current switches may be sensitive to thermal history and produce an effect known as 'intersymbol interference'). That is, if the latch has been switched to one state for a sufficient period of time, one transistor heats more than the other and changes its switch threshold. When the signal driving the switch has a non-zero risetime, this has the effect of changing the timing of the switch transition. Such thermal errors are difficult to characterize and compensate for.
>
> Traditional approaches for suppressing intersymbol interference include a return-to-zero (RZ) configuration where the DAC current is gated off during part of each clock cycle. However, this requires faster operation of the DAC switch, adds another data edge that is subject to clock jitter, and produces a much less smooth output.
>
> More recently, Adams *et al.* described a scheme with two interleaved RZ DACs to provide a more continuous output than does a single RZ DAC. (See "A 113dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling", IEEE Solid-State Circuits Conference, 1998.) This approach consumes additional current, is subject to clock jitter, and does not cancel all thermal effects.

* * *

> Inasmuch as the ADC is typically used in continuous time feedback loop, the timing errors become errors in the analog signals output from the ADC."

Hence, a need has remained in the art for a precise switch for use in a continuous time sigma-delta or delta-sigma modulator. Specifically, there is a need for a switch that does not generate timing errors due to clock jitter.

The present invention addresses this need by providing a switch in which the inputs are allowed to settle to a full logic value before current is switched to the emitters of each differential pair thereof. This prevents slight variations in timing from influencing the output. (See the disclosure with respect to Figure 1 generally and specifically Figure 2 on pages 6 and 7 of the present application.)

The invention is set forth in Claims of varying scope of which Claim 56 as amended is illustrative. Claim 56 now recites:

> 56. A delta-sigma modulator comprising:
> a loop filter;
> a comparator coupled to the loop filter; and
> a switch, coupled to said comparator and said filter, said switch comprising:
> first means for providing a first set of first and second complementary intermediate signals;
> second means for providing a second set of third and fourth complementary intermediate signals;
> third means responsive to the first set of signals for providing complementary output signals;
> fourth means responsive to the second set of signals for providing complementary output signals; and
> **fifth means for clocking said first means and said second means to apply said first set of signals to said third means on a first edge of a clock pulse and apply said second set of signals to said fourth means on a second edge of said clock pulse.** (Emphasis added.)

See also new Claim 85 which recites:

85. A delta-sigma modulator comprising:
a loop filter;
a comparator coupled to the loop filter;
a master latch coupled to said comparator for providing a first set of first and second complementary intermediate signals;
a slave latch coupled to said master latch for providing a second set of third and fourth complementary intermediate signals;
a first differential pair of transistors responsive to the first set of signals for providing a first set of complementary output signals;
a second differential pair of transistors responsive to the second set of signals for providing a second set of complementary output signals; and
means for switching current through said first differential pair of transistors and said second differential pair of transistors after the inputs thereof have settled to a full logic value. (Emphasis added.)

None of the references, taken alone or in combination, teach, disclose or suggest the invention as presently claimed. That is, none of the references, teach, disclose or suggest a delta-sigma modulator having means for switching current through differential pairs of transistors thereof after the inputs thereto have settled to a full logic value.

In accordance with the illustrative embodiment, this is effected by clocking signals from master and slave latches on the leading and trailing edge of a **single** clock pulse.

This is not taught by Cake inasmuch as the switch of Cake is designed to operate on time interleaved pulses at $f_x/2$ at angle '0' radians and $f_x/2$ at angle 'π' for the first and second latches thereof. (See Fig. 6.) Hence, Cake is adapted to operate on separate samples to achieve a high sampling rate of f_s. Cake is not adapted to operate on a **single** sample of data. More importantly, no teaching is provided with respect to an arrangement for minimizing jitter by allowing the inputs to the differential pairs of transistors to settle before switching.

The shortcomings of Cake are not addressed by the teachings of Cheng and Watson.

Accordingly, the Claims are presented as properly defining an invention patentable over the prior art. Reconsideration, allowance and passage to issue are respectfully requested.

Respectfully submitted,
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